Scaling of Back End of Line Processing : Opportunities and Challenges

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Back End Of Line (BEOL) processing has an ever increasing impact on the whole of integrated circuit manufacturing. Its influence on the delay of the signals is for some nodes higher than the Front End of Line Processes. Moreover, for the more advanced nodes, the back end cost will be as high or higher than the front end cost. A huge part of the complexity and cost of IC processing is due to complicated solutions needed for the lithography: Litho-Etch-Litho-Etch (LELE), Self-Aligned Double (and Quadruple) Patterning (SAD(Q)P) and also Extreme UV (EUV) lithography are discussed. Advanced dielectrics offer opportunities but also immense challenges for integration. Self-Aligned Molecules (SAMs) may offer solutions by sealing off the pores of the low-k dielectrics. New metal barrier-liner combinations are being introduced and other materials replacing Cu for very narrow metal line metallization, are investigated. Time Dependent Dielectric Breakdown (TDDB) and Electromigration challenges and possible solutions will also be discussed.

Biography

Patrick Verdonck obtained his Electrical Engineering degree in 1981 at the Katholieke Universiteit Leuven, Belgium, and his Ph.D. in Electrical Engineering in 1994 at the UNICAMP, Brazil. Before joining imec in 2005, he worked for approximately 20 years at the Universidade de Sao Paulo, Brazil. He is co-author on a book on characterization of microelectronic technologies (in Portuguese) and author and co-author of more than 200 technical papers. His main interests are in plasma processing for microelectronics, mainly PECVD and etching, and in low-k and dielectric barrier materials and their integration in advanced integrated circuits.