A Differential Cyclic Analog-to-Digital Converter for Energy Meter Systems

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1. Abstract

In this paper, a differential cyclic analog-to-digital converter based in switched-capacitor techniques is presented. This approach allows a reduced die size and achieves a higher precision, making this circuit suitable to low speed measurements, such electric energy meter systems where a minimum sampling rate of 1,200 samples per second is required for 2-channel systems (single-phase) and 7,600 samples per second for three-phase systems.

The ADC fabricated in AMS 0.35µm digital CMOS integration process can achieve a 10-bit resolution at 7.6k samples per second conversion rate and occupies 0.36 mm² silicon area.

2. Introduction

Cyclic analog-to-digital converters (ADCs) are used in moderate-to-high-accuracy and low-to-moderate-frequency applications, especially where low power consumption and low area occupation is required [1], [2]. In a cyclic ADC, the residue signal is cyclic, thus only one stage is needed, and N periods are required to convert an N-bit digital code. In these ADCs, noise and accuracy requirements decrease from the most-significant bit (MSB) to the least-significant bit (LSB) cycle, but the invested energy per cycle is “conventionally” constant [2]. The main disadvantage of this mode of operation is the long conversion cycles, which is exacerbated by the need to use closed-loop amplifiers instead of comparators [2].

The basic principle of static meters, based on the analog-to-digital conversion of current and voltage signals, is the application of suitable metrics and algorithms that take into account real voltage and current harmonic contents [3]. This work presents a compact cyclic analog-to-digital converter suitable to applications where the sampled voltage and current at a power line are converted to digital and stored for further digital processing (calculation of electrical quantities such as instantaneous power, power factor, harmonic distortion, etc.).

3. Cyclic Analog-to-Digital Converter

A. Cyclic Conversion Algorithm

The cyclic analog-to-digital conversion comprises the execution of an algorithm that includes operations such as comparison, multiplication by two and subtraction. A conceptual illustration of the cyclic A/D conversion for offset binary coding is shown in Fig. 1(a) [4]. At the beginning of the conversion cycle, the input signal is compared to the reference voltage $V_{REF}$. If the input signal is greater than $V_{REF}$ value, the MSB is set to one and the reference voltage value is subtracted from the input voltage. The remaining value is multiplied by two and used as the input signal on the next cycle, where the next output bit will be calculated. If the input signal is smaller than $V_{REF}$, the corresponding bit is set to zero and the present input value is doubled and recirculated to the input in order to obtain the next output bit. The conversion continues until the desired number of bits has been obtained.

B. Differential Cyclic Analog-to-Digital Converter

The cyclic ADC circuit is implemented by the two-stage differential circuit depicted in Fig. 1(b). The switches numbered from 1 to 10 are implemented by MOS transistors with dummy elements in order to prevent charge injection. Each output bit is available after three cycles of clock and the switching sequence that performs the analog-to-digital conversion is depicted in Table I. The next switching sequence depends on the value of the previous converted bit $B(i)$. At the beginning of the conversion cycle, operation (I) is performed and the MSB is obtained.

Table I. ADC switching sequence for each output bit.

<table>
<thead>
<tr>
<th>Switch</th>
<th>(I) MSB</th>
<th>(II) $B(i) = 1$</th>
<th>(III) $B(i) = 0$</th>
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</thead>
<tbody>
<tr>
<td>1</td>
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<td>10</td>
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</tbody>
</table>

C. Fully-Differential Folded Cascode OTA

A fully-differential folded cascode OTA with capacitive common-mode feedback circuit (CMFB) has been implemented in this converter [5]. This topology is largely used due to its simplicity, symmetry, speed, lower power consumption and improved PSRR in spite its limited output voltage range, when compared to a two-stage amplifier [6]. The implemented amplifier presented an open-loop gain of 85.4dB, a phase margin of 82.2 degrees and a 0-dB frequency of 52.3MHz.
Fig.1. (a) Analog-to-digital conversion sequence; (b) Implemented Analog-to-digital cyclic converter.

4. Simulation Results

The implemented circuit was simulated using a 60Hz/3.5Vpp sinusoidal signal as input voltage with offset equal to 1.75Vdc. The circuit was designed to work with a 5-Vdc supply voltage and V_{REF} is set to half scale of the input signal (1.75Vdc). With a 10-bit resolution, there will be 1024 possible digital words at the output. The results showed only 10 wrong values, deviated by ± 1LSB from the correct value. Fig.2 shows the implemented circuit, comprised by two OTAs, MOS switches, matched capacitors and digital control circuitry. Mentor Graphics’ IC Station tools were used to implement and simulate the circuit using AMS CMOS 0.35µm design kit. The circuit occupied an area of 0.36 mm².

Fig.2. Circuit implemented in AMS 0.35 µm technology.

5. Conclusions

This work presented a differential cyclic analog-to-digital converter suitable to low-frequency operation. The use of this topology saves a significant amount of silicon area once the circuit size is independent of the number of converting bits. Differential topology improved the circuit precision once the clock feedthrought and the charge injection effects on the MOS switches are minimized. Simulation showed a maximum deviation of ± 1LSB in only 10 values, among the 1024 possible output values for a 10-bit resolution. The circuit was implemented in a 0.35µm process and occupied an area of 0.36 mm².

References