Integração de Processo de Microeletrônica

Exemplo: processo nMOS com:

- porta Si-poli
- isolação LOCOS

Litografia: de máscara à gravação

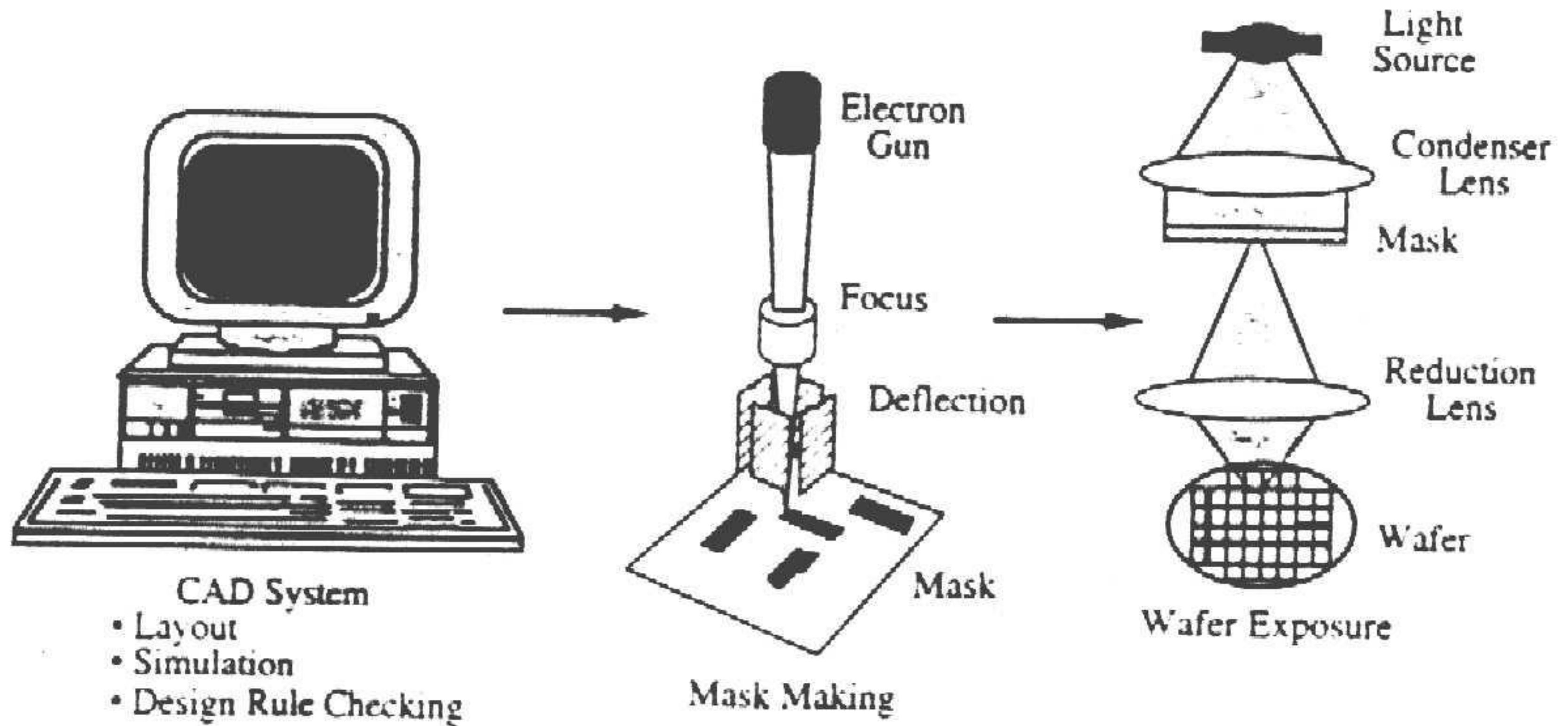
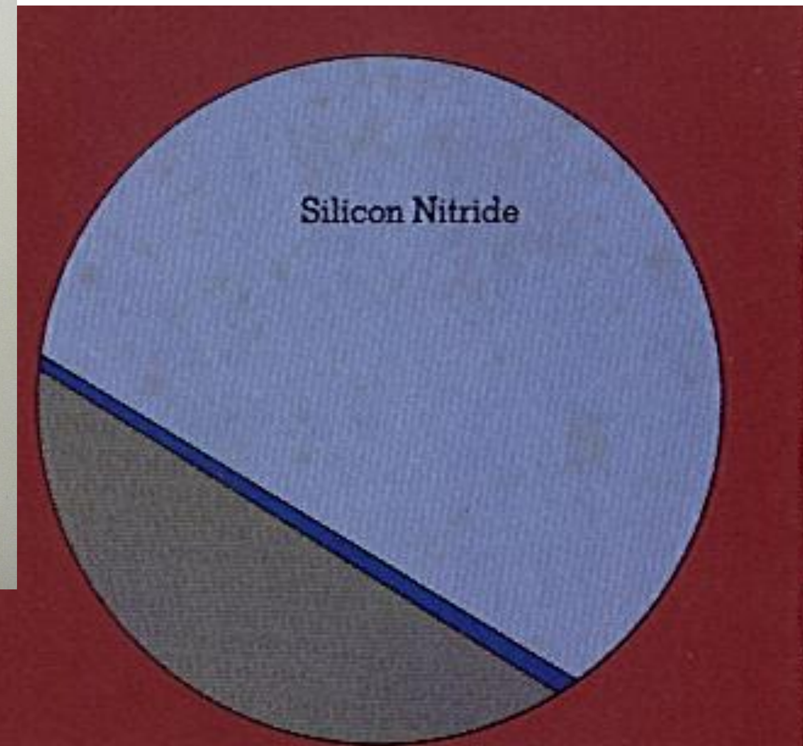


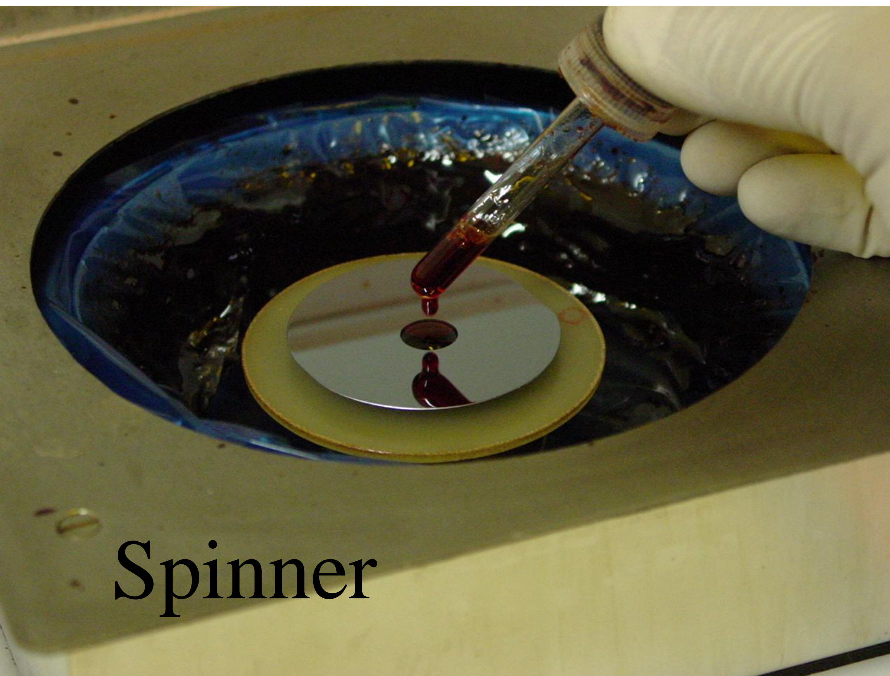
Figure 5–1 Lithography process from mask design to wafer printing.

Deposição de camada de Si_3N_4 por CVD



Ex.: $SiH_4 + N_2$

Aplicação e espalhamento de fotorresiste



2

Photoresist

Photoresist Coating

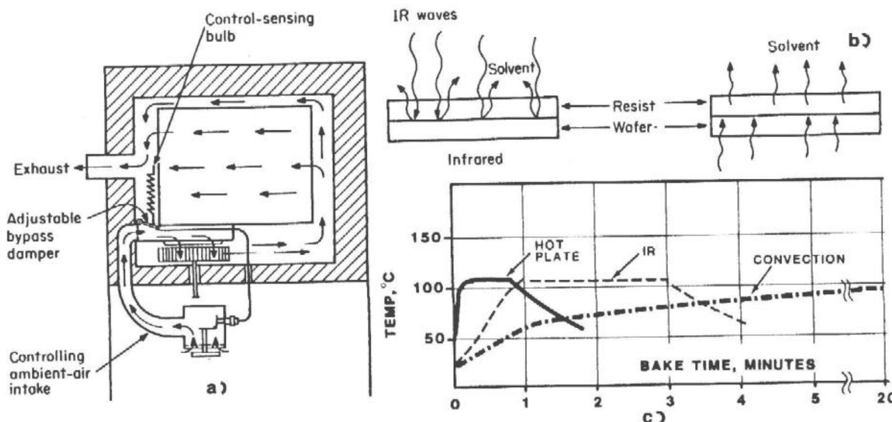
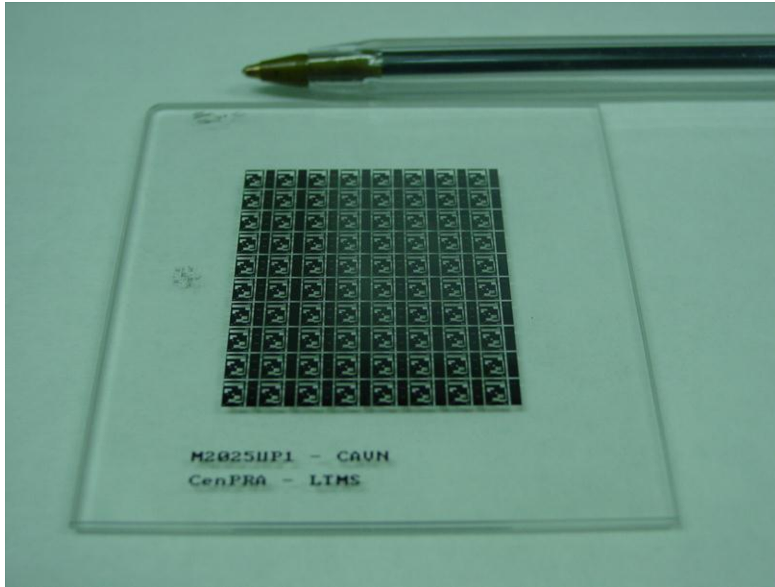
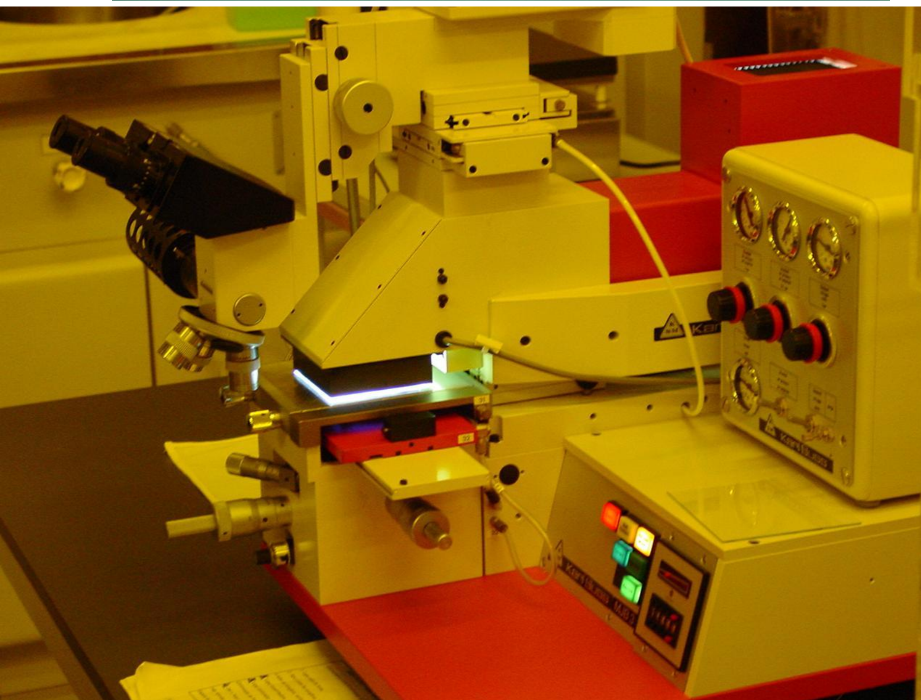


Fig. 20 (a) Convection oven cross section. Courtesy of Blue M, a Unit of General Signal. (b) Infrared and conduction solvent removal mechanisms. (c) Profiles for various bake methods[45]. Reprinted with permission of the Eaton Corporation.

Alinhamento da Máscara e Exposição



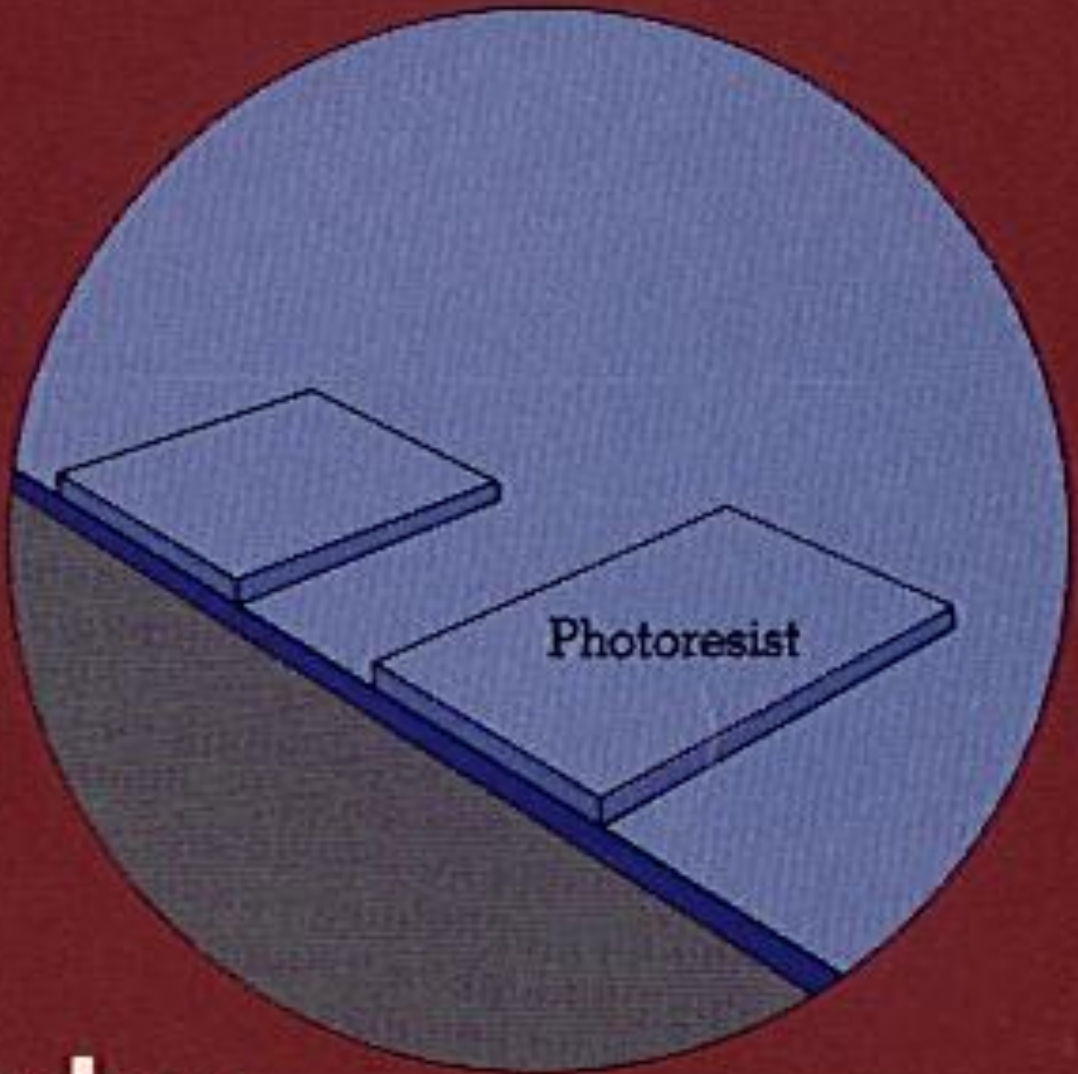


Mask

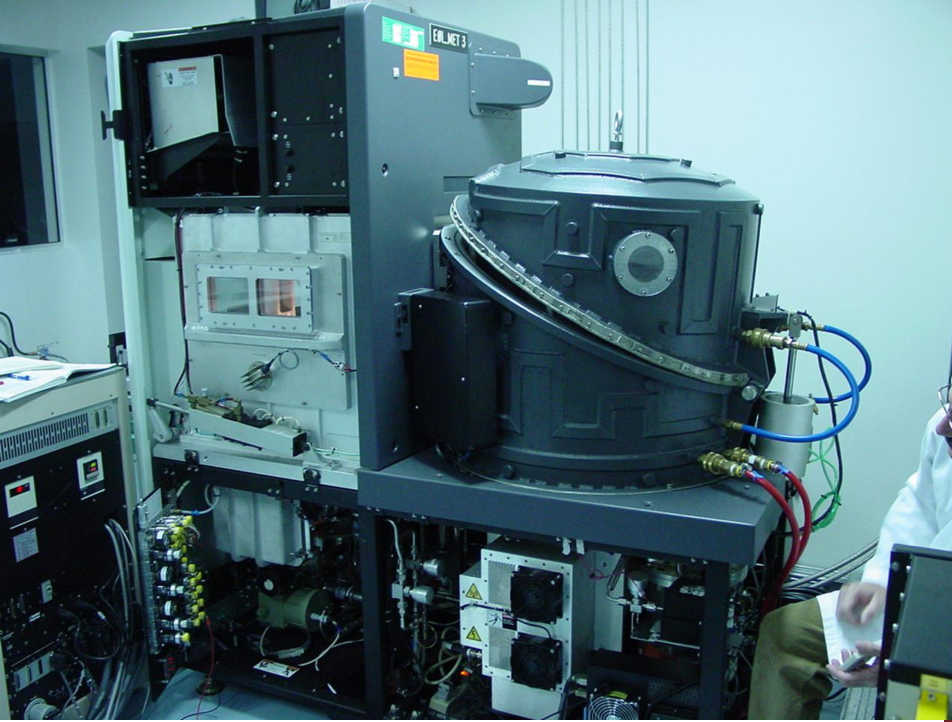
3

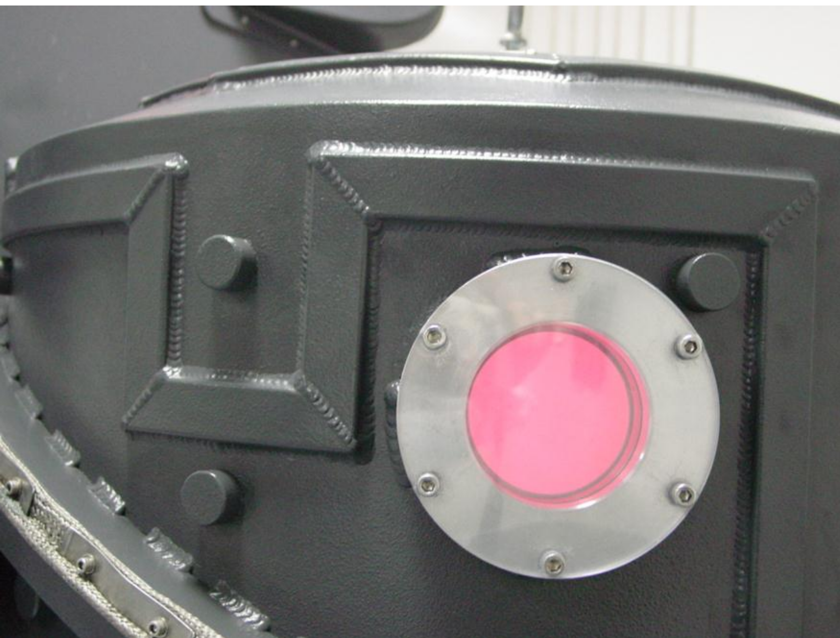
Photolithography

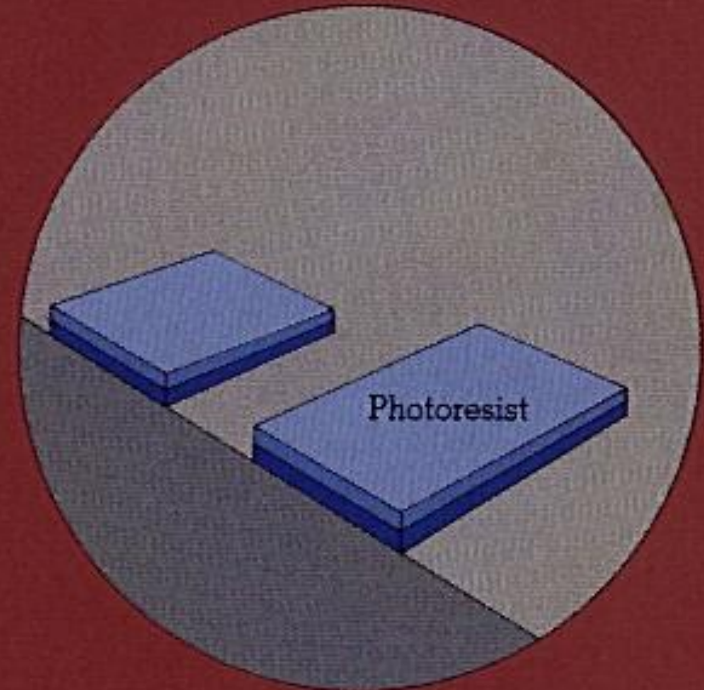
Revelação do Fotorresiste



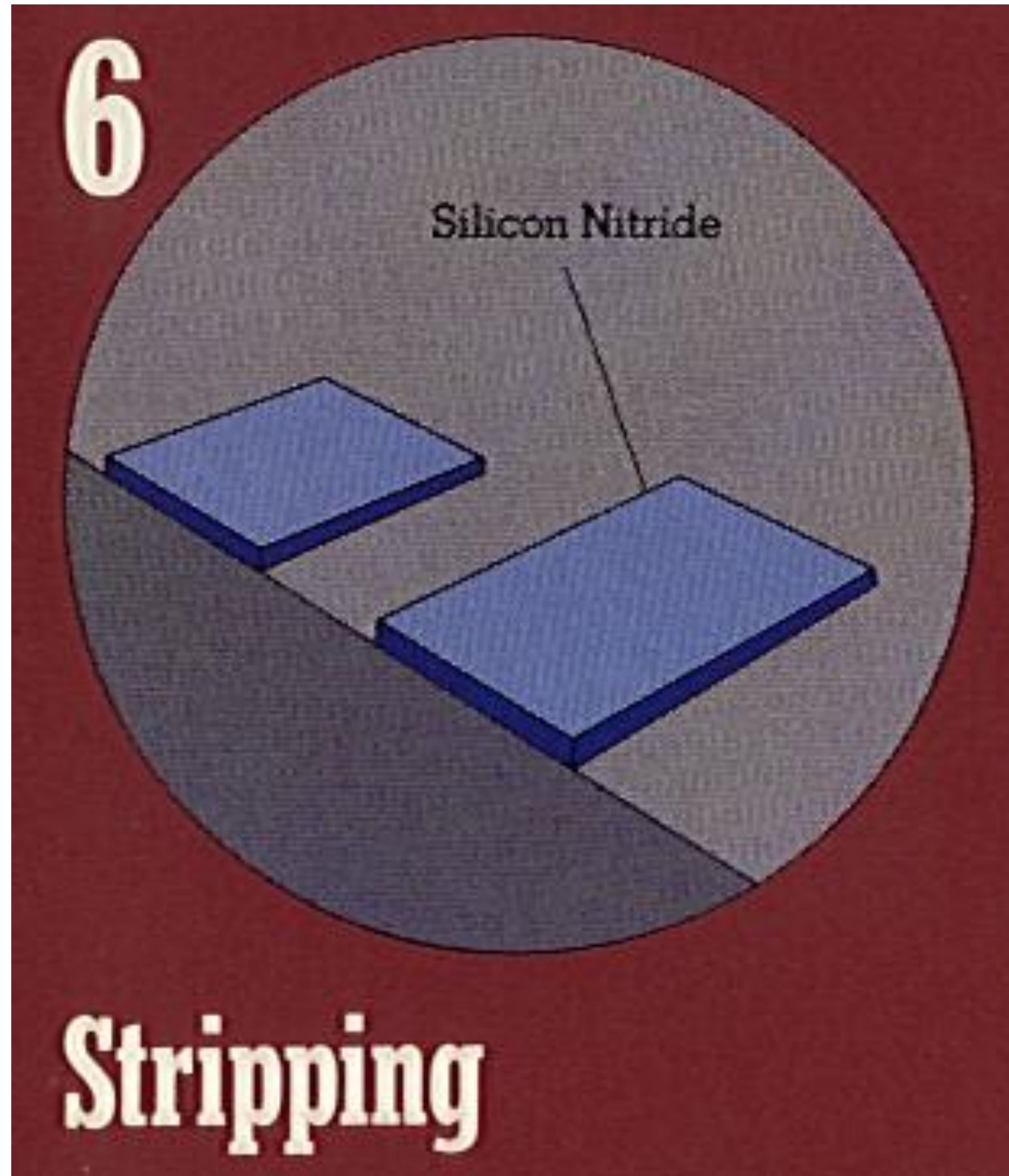
Corrosão do Si_3N_4 por plasma reativo





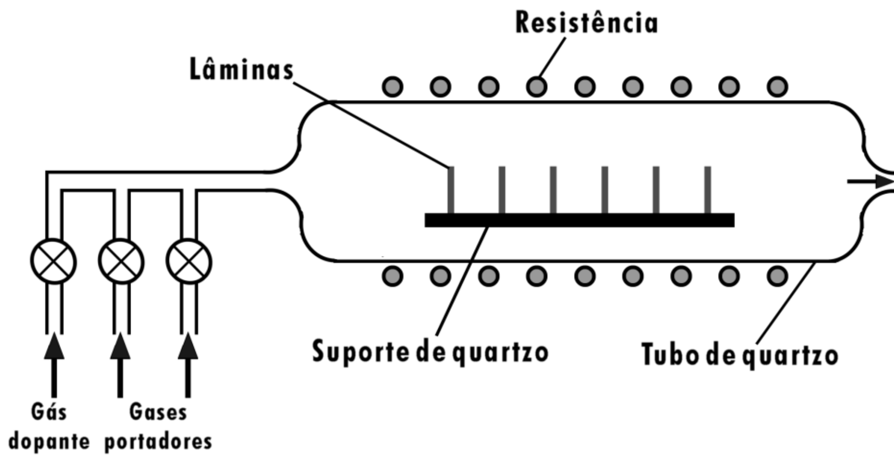


Remoção do fotorresiste por dissolução em acetona



Oxidação do Si em Forno Térmico

Ex.: 1000 °C em $O_2 + H_2O$



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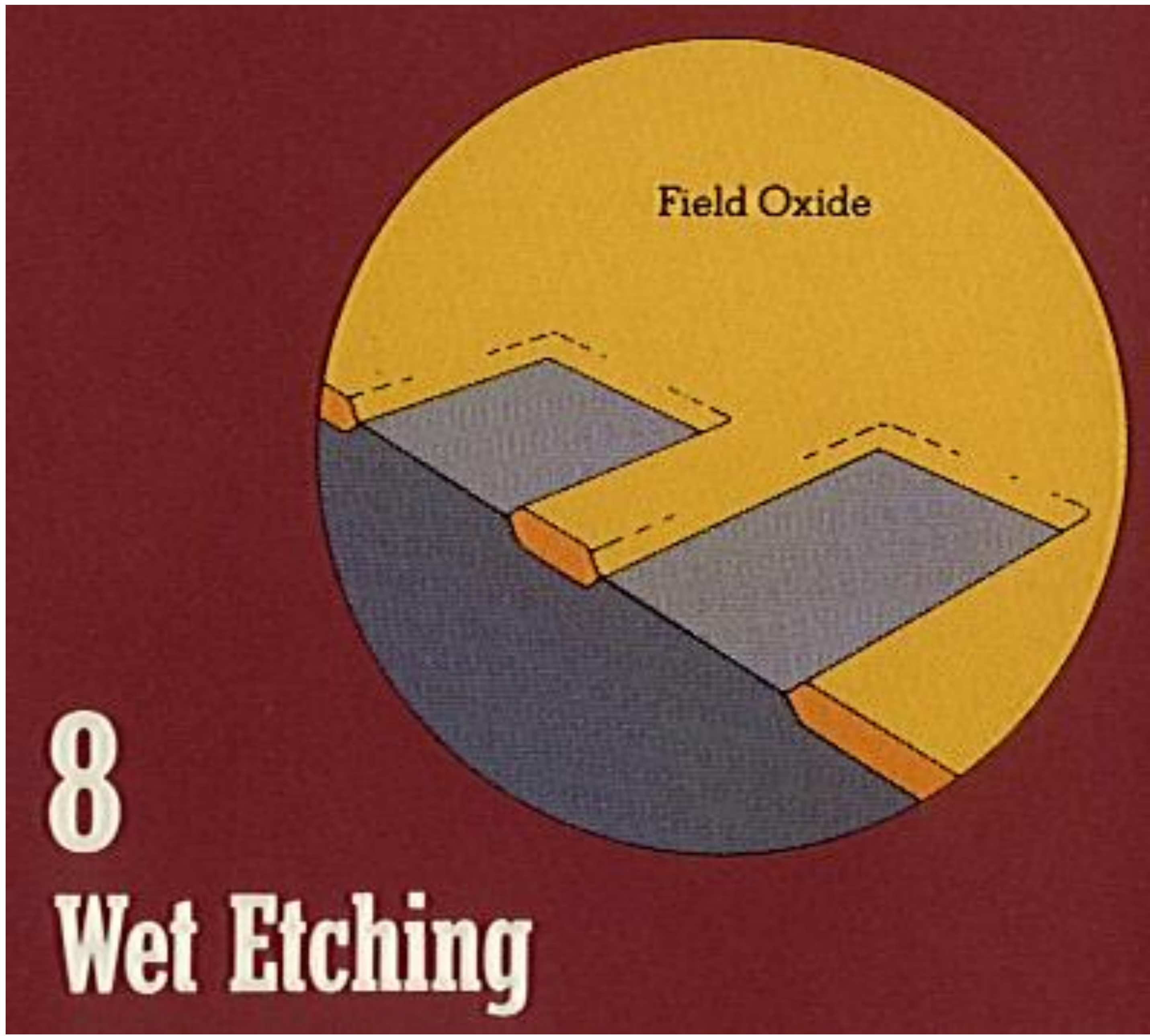
Field Oxide

Silicon Nitride

Field Oxidation

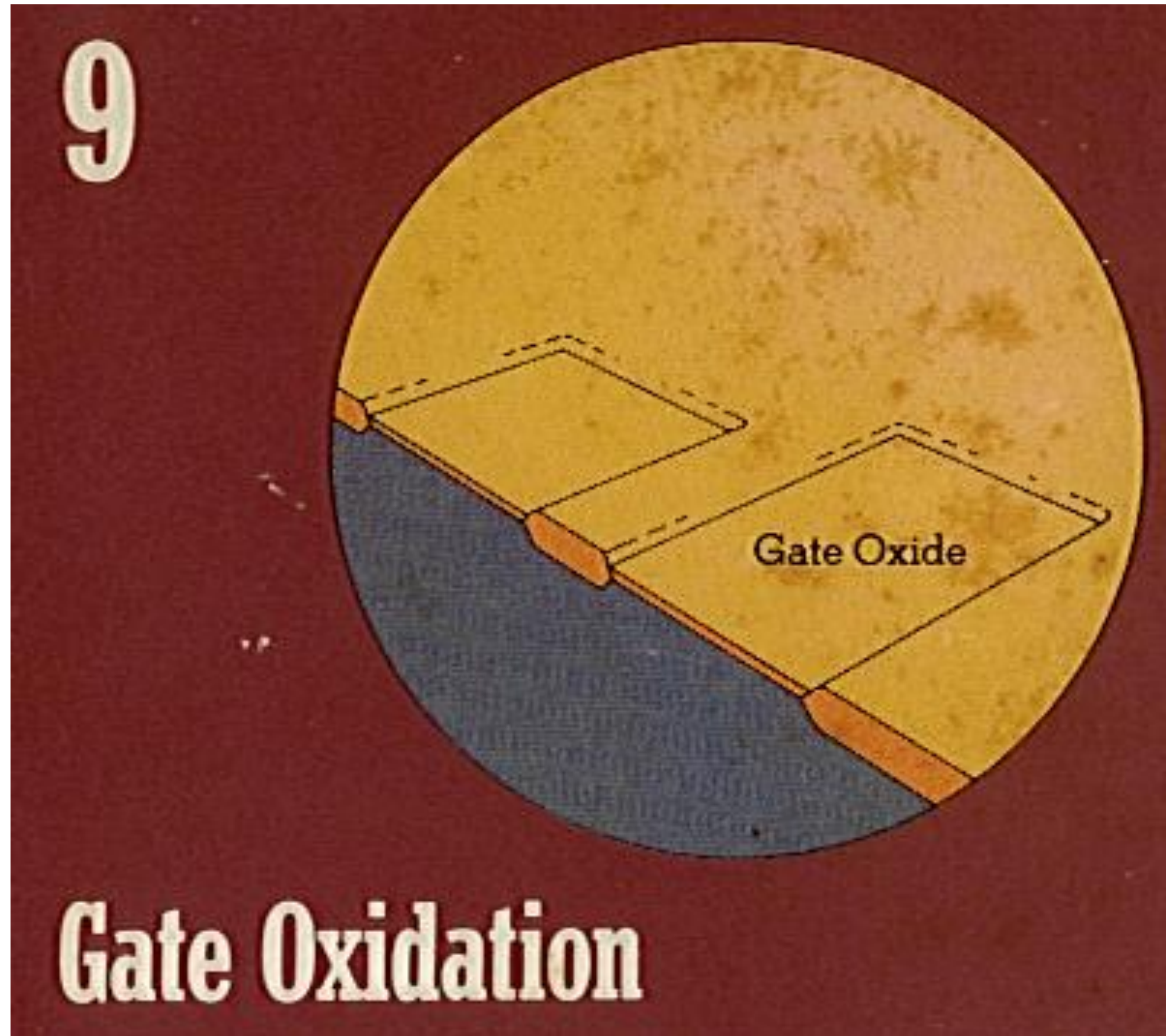
Corrosão da camada de Si_3N_4 em H_3PO_4



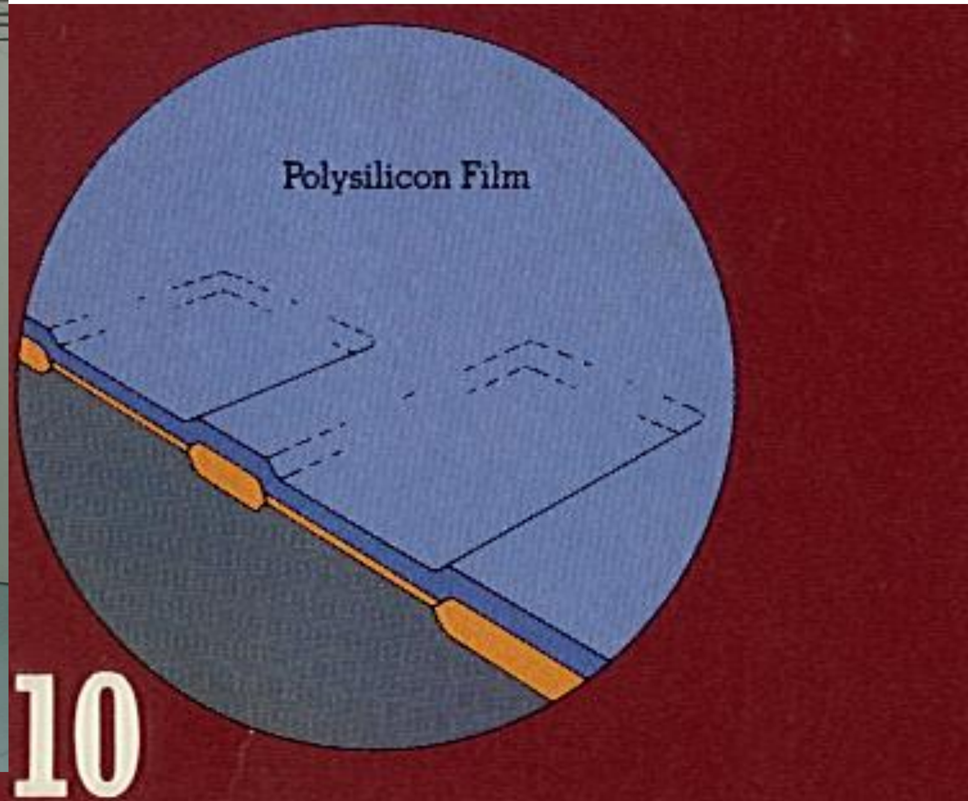
Oxidação do Si em Forno Térmico

Óxido Fino
de 2 a 50 nm

Ex. 900 °C
em O_2

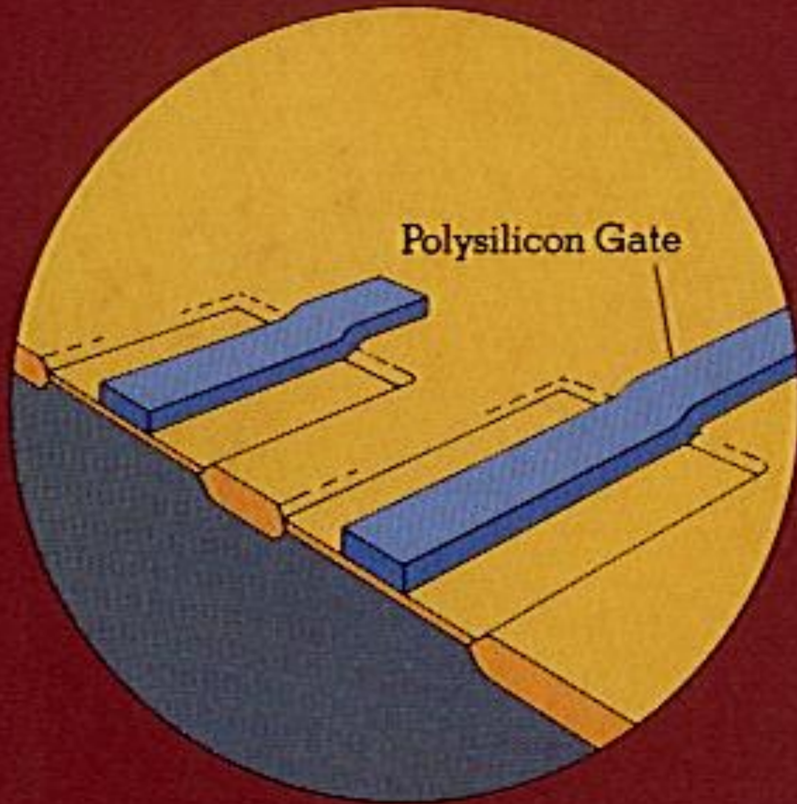


Deposição de camada de Si-poli por CVD



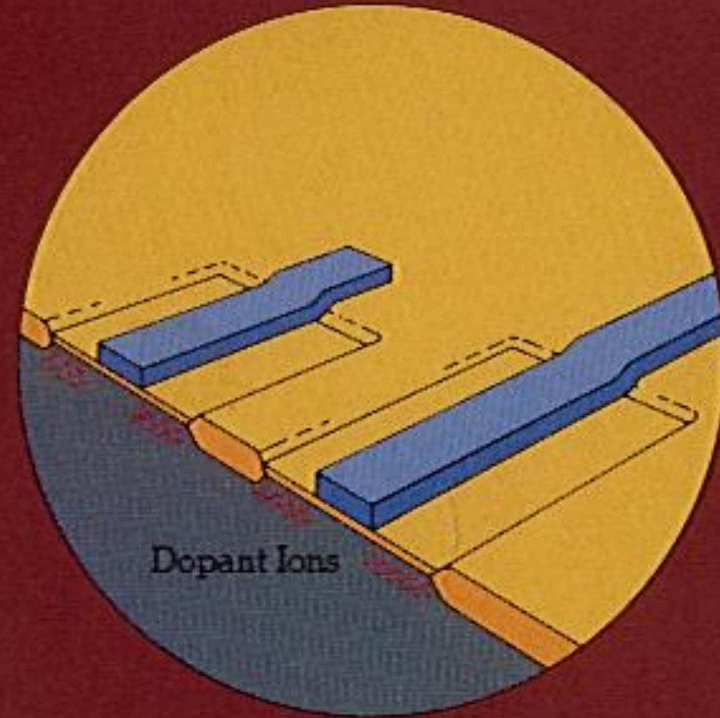
Ex. 650 °C em SiH_4

Fotolitografia e corrosão da camada de Si-poli por plasma reativo



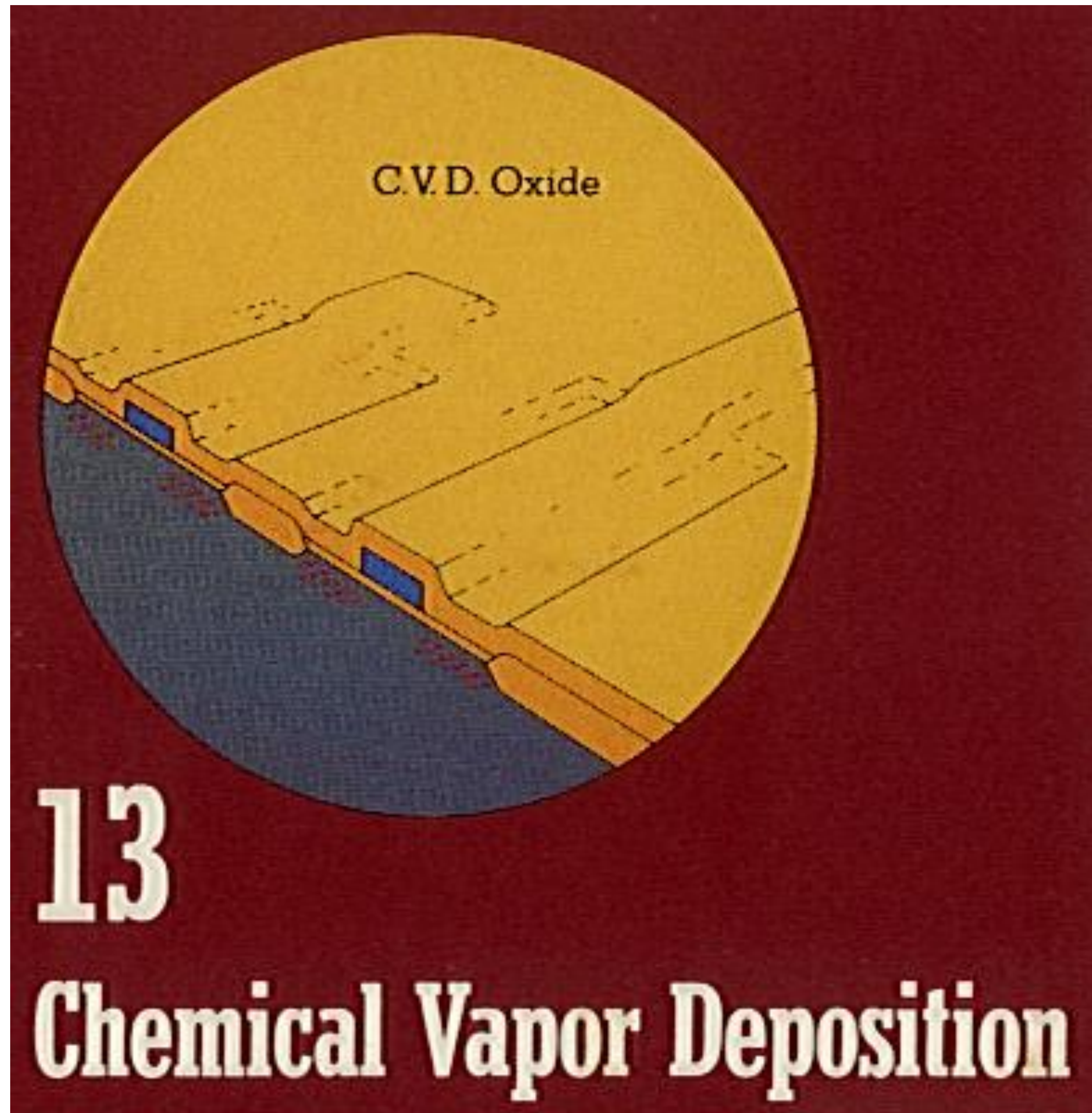
Formação de Fonte/Dreno por Implantação de Íons

Ex.: íons de fósforo a 50 keV, $10^{16}/cm^2$

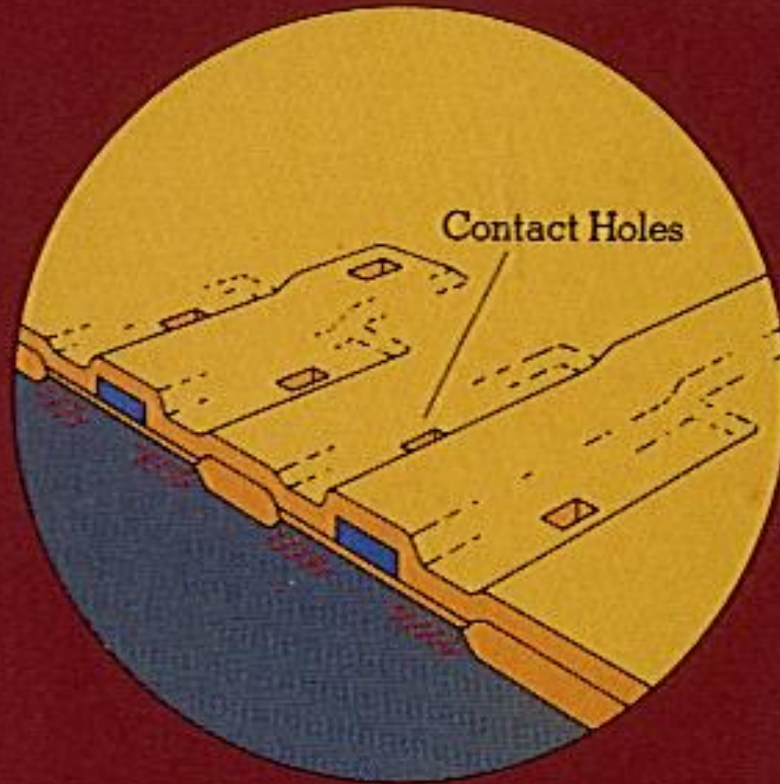


Deposição de camada de SiO_2 por PECVD

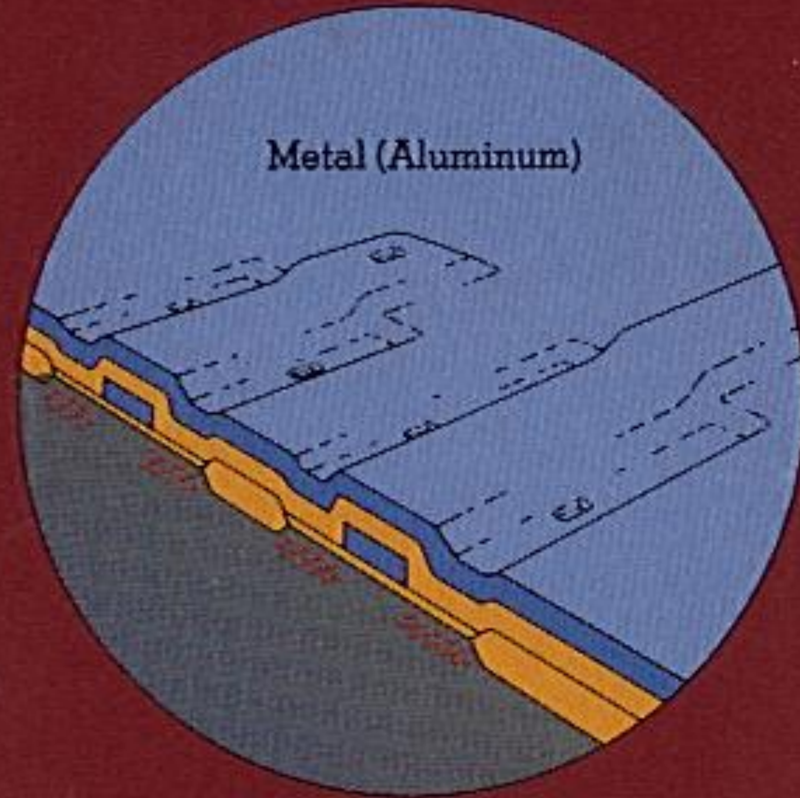
Ex.: a 400 °C em
$SiH_4 + N_2O$



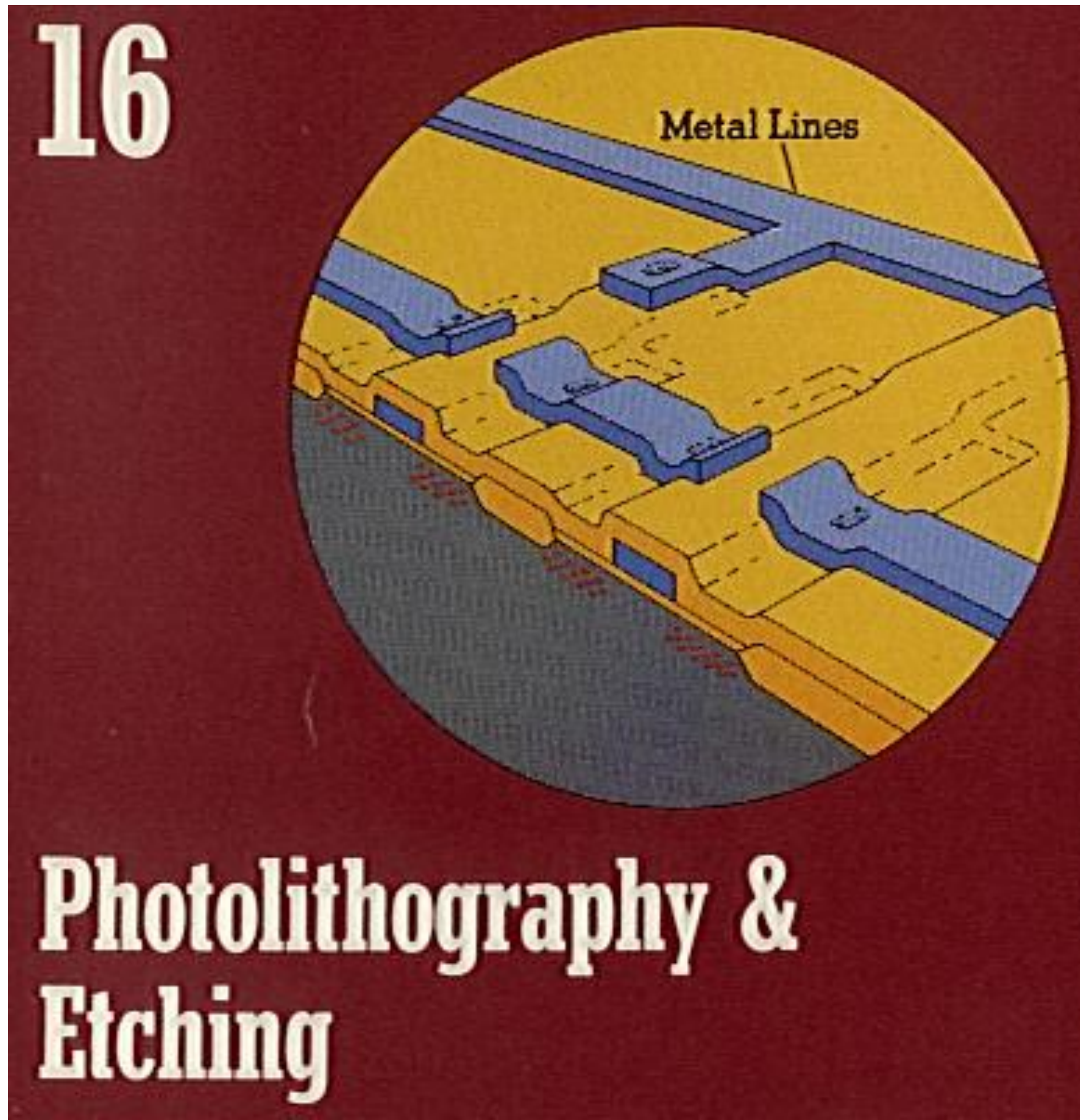
Fotolitografia e corrosão da camada de SiO_2 por plasma reativo

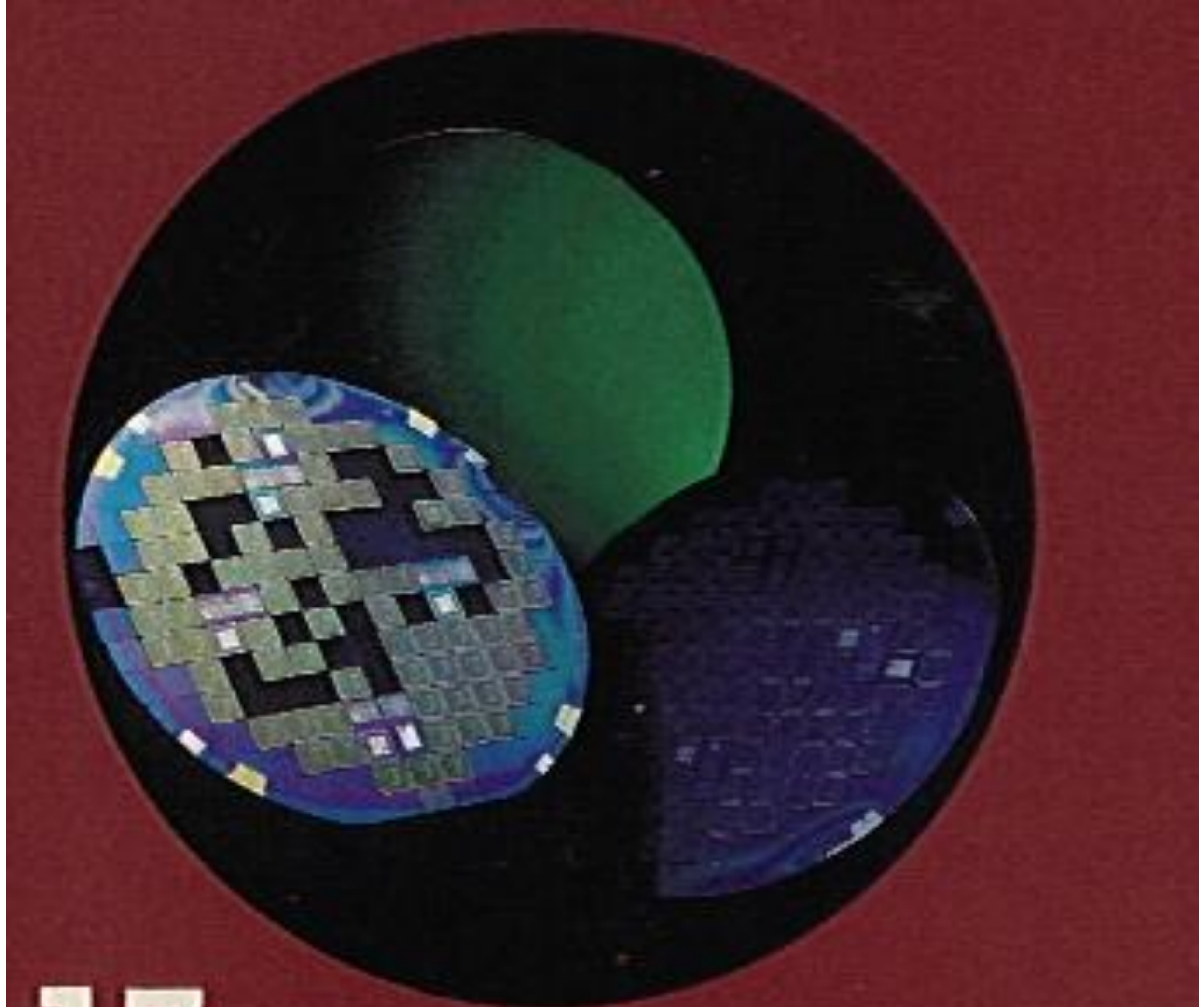


Deposição de camada de Alumínio por evaporação térmica ou por “sputtering”.



Fotolitografia e corrosão da camada de Alumínio por plasma reativo





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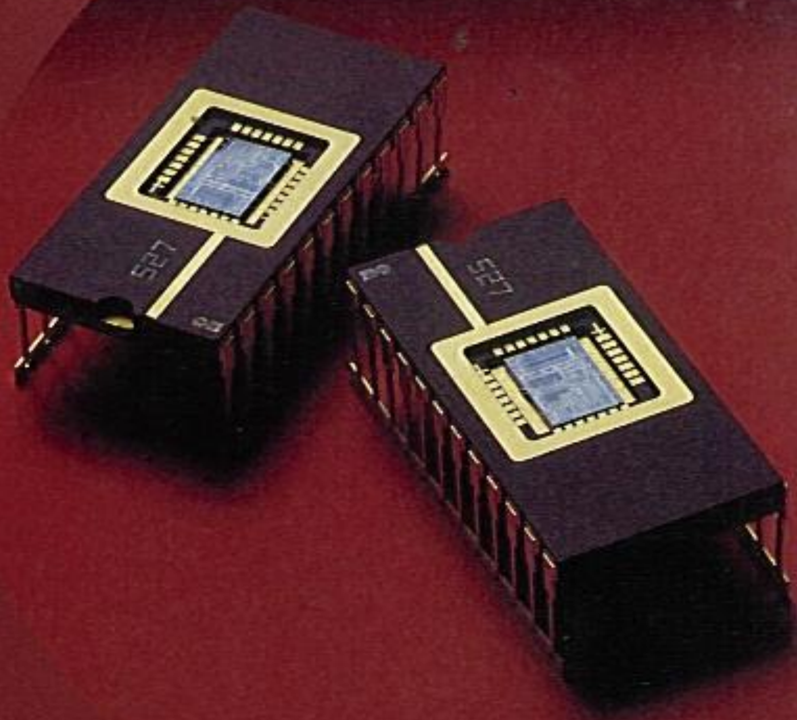
Testing & Wafer Dicing



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Wire Bonding & Packaging